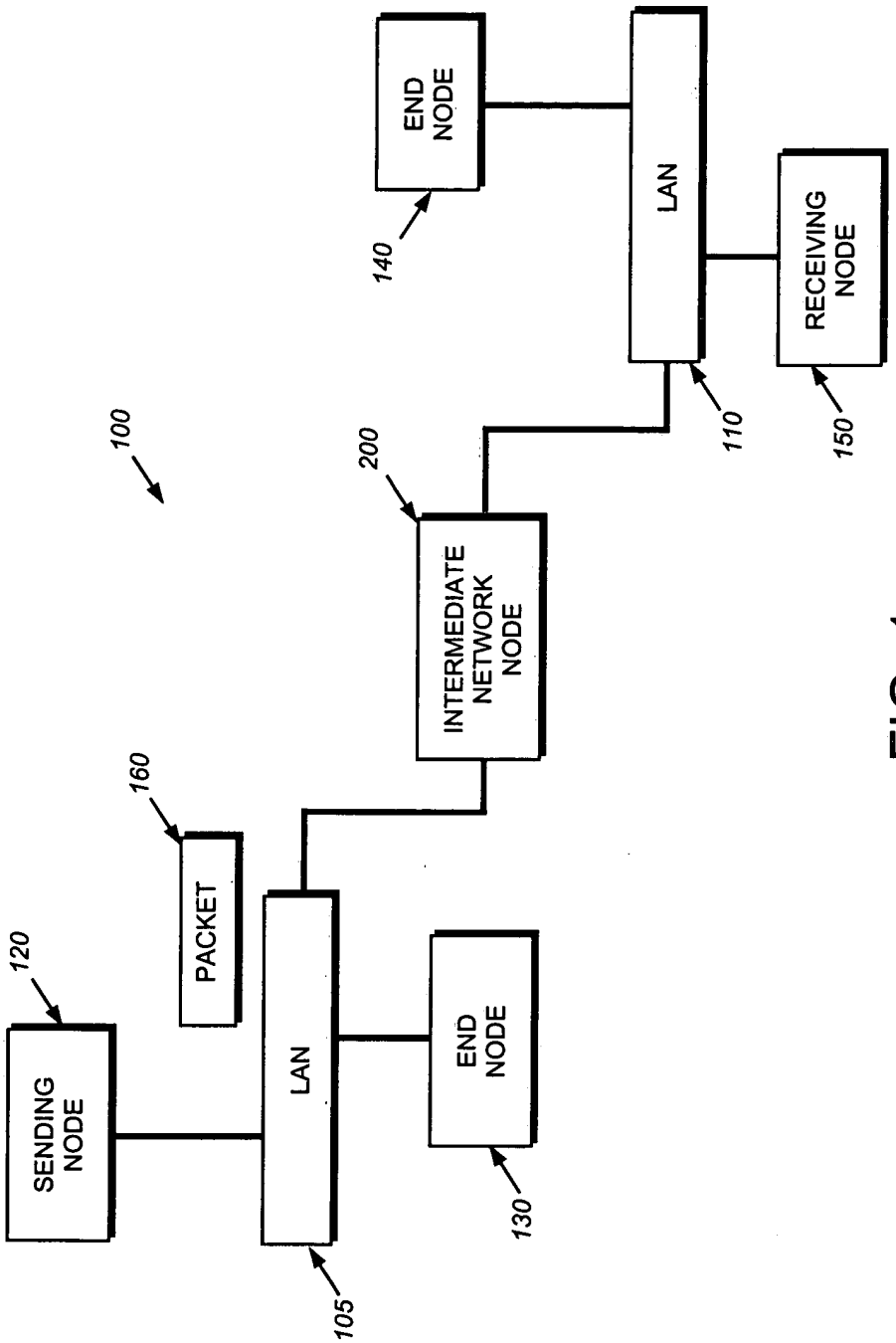

100
SENDING NODE
120
PACKET
160
LAN
105
END NODE
130
INTERMEDIATE NETWORK NODE
200
LAN
110
END NODE
140
RECEIVING NODE
150

FIG. 1

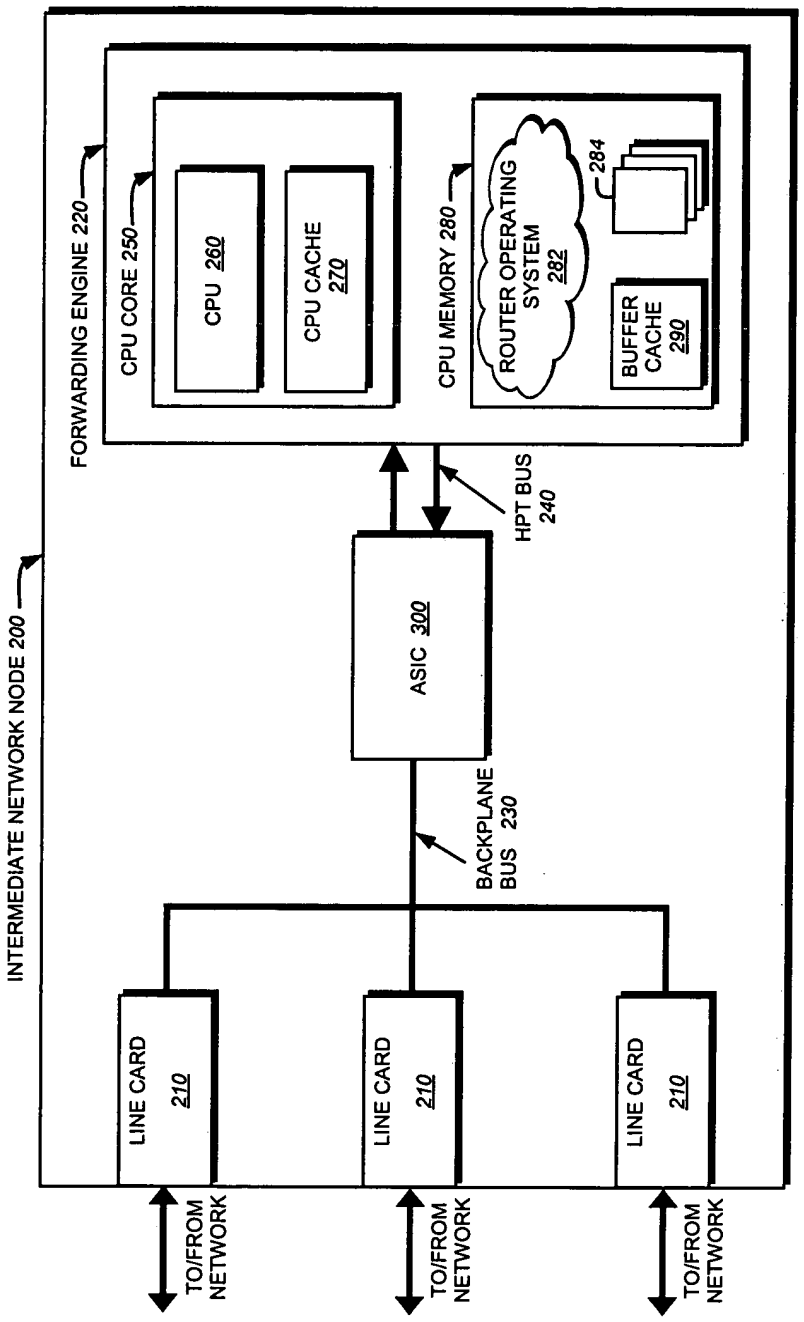

INTERMEDIATE NETWORK NODE 200
FORWARDING ENGINE 220
CPU CORE 250
CPU 260
CPU CACHE 270
CPU MEMORY 280
ROUTER OPERATING SYSTEM 282
284
BUFFER CACHE 290
HPT BUS 240
ASIC 300
BACKPLANE BUS 230
LINE CARD 210
LINE CARD 210
LINE CARD 210
TO/FROM NETWORK
TO/FROM NETWORK
TO/FROM NETWORK

FIG. 2

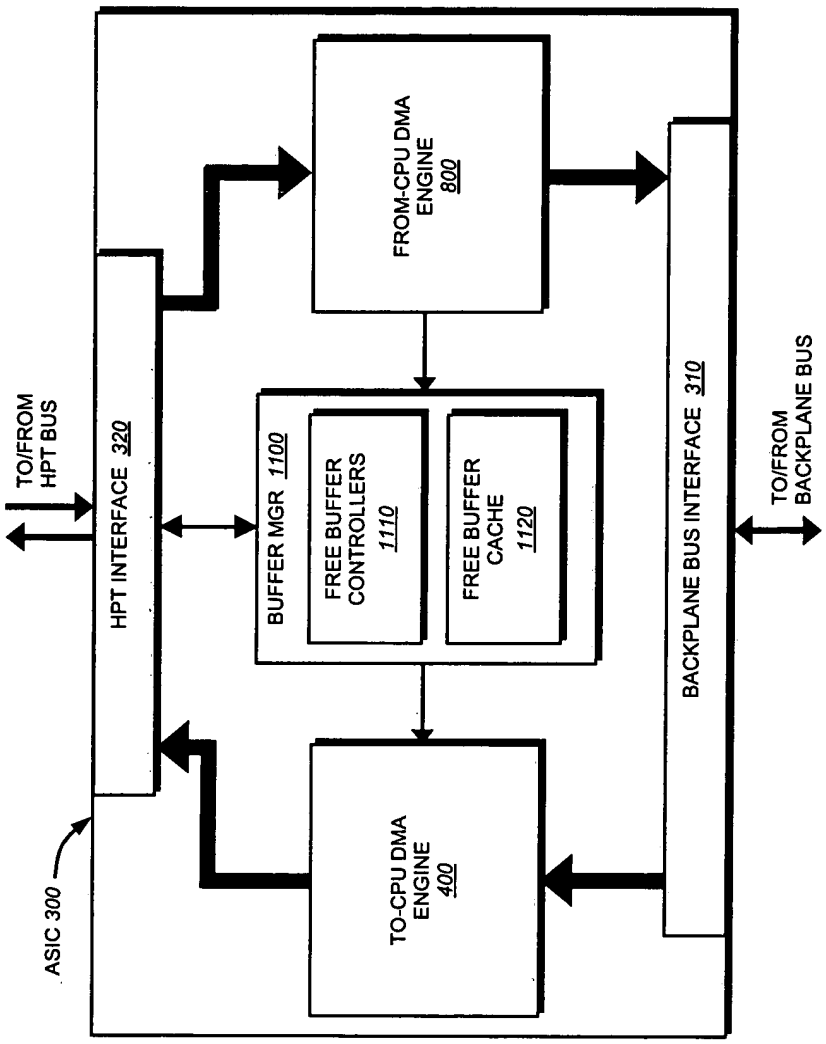

TO/FROM HPT BUS
HPT INTERFACE 320
FROM-CPU DMA ENGINE 800
BUFFER MGR 1100
FREE BUFFER CONTROLLERS 1110
FREE BUFFER CACHE 1120
BACKPLANE BUS INTERFACE 310
TO/FROM BACKPLANE BUS
TO-CPU DMA ENGINE 400
ASIC 300

FIG. 3

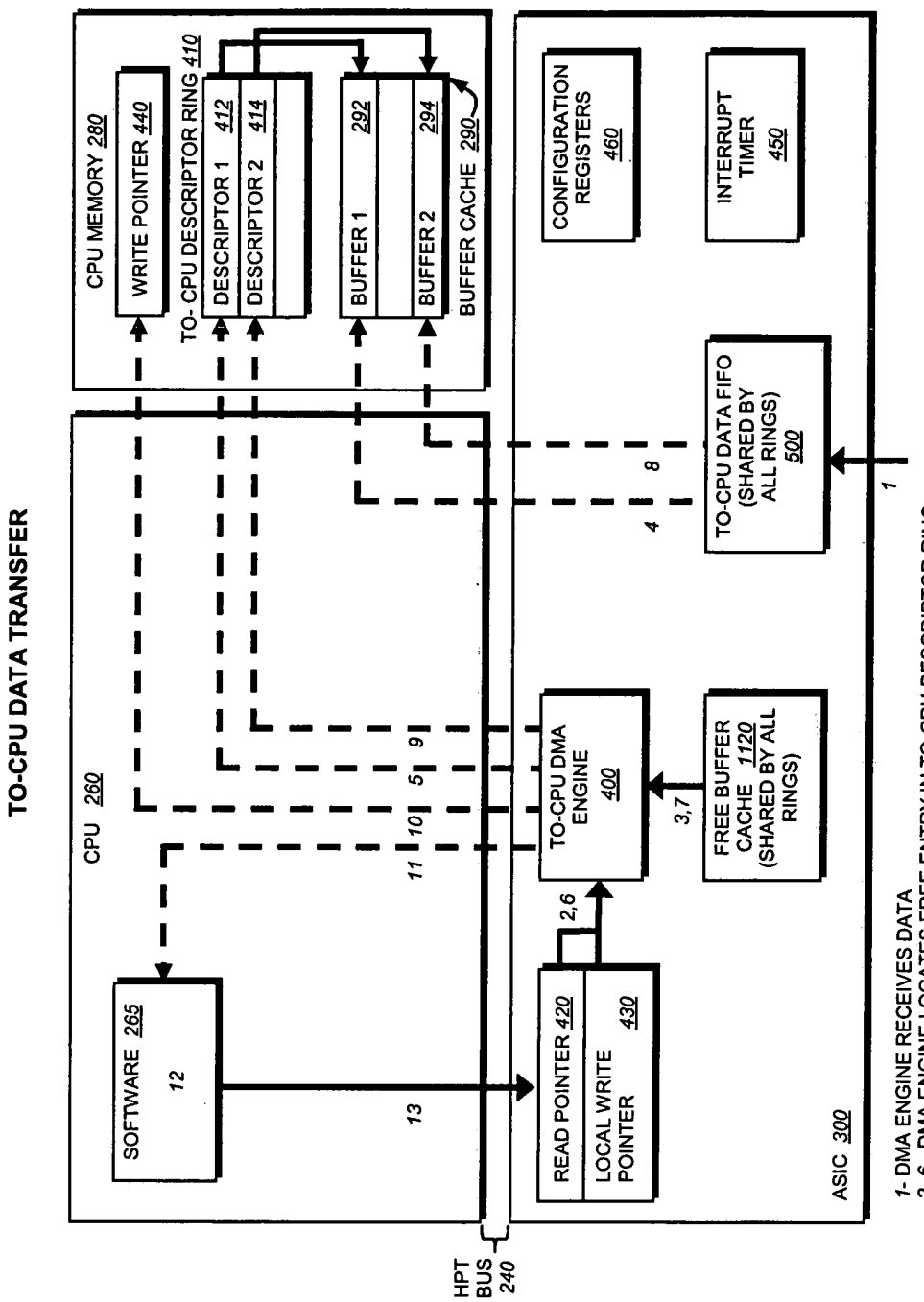

TO-CPU DATA TRANSFER
CPU MEMORY 280
WRITE POINTER 440
TO- CPU DESCRIPTOR RING 410
DESCRIPTOR 1 412
DESCRIPTOR 2 414
BUFFER 1 292
BUFFER 2 294
BUFFER CACHE 290
CONFIGURATION REGISTERS 460
INTERRUPT TIMER 450
TO-CPU DATA FIFO (SHARED BY ALL RINGS) 500
CPU 260
SOFTWARE 265
12
13
11
10
5
9
TO-CPU DMA ENGINE 400
2,6
3,7
FREE BUFFER CACHE 1120 (SHARED BY ALL RINGS)
READ POINTER 420
LOCAL WRITE POINTER 430
ASIC 300
HPT BUS 240
4
8
1
1- DMA ENGINE RECEIVES DATA
2, 6 - DMA ENGINE LOCATES FREE ENTRY IN TO-CPU DESCRIPTOR RING
3, 7- DMA ENGINE GETS FREE BUFFER DESCRIPTOR
4, 8- DMA ENGINE WRITES DATA FROM TO-CPU DATA FIFO TO BUFFER
5, 9- DMA ENGINE WRITES DESCRIPTOR TO TO-CPU DESCRIPTOR RING
10- DMA ENGINE WRITES WRITE POINTER AFTER INTERRUPT TIMER EXPIRES
11- DMA ENGINE WRITES INTERRUPT AFTER ALL THE PACKET'S DESCRIPTORS ARE WRITTEN TO THE TO-CPU DESCRIPTOR RING
12- SOFTWARE PROCESSES PACKET
13- SOFTWARE WRITES READ POINTER TO FREE DESCRIPTOR

FIG. 4

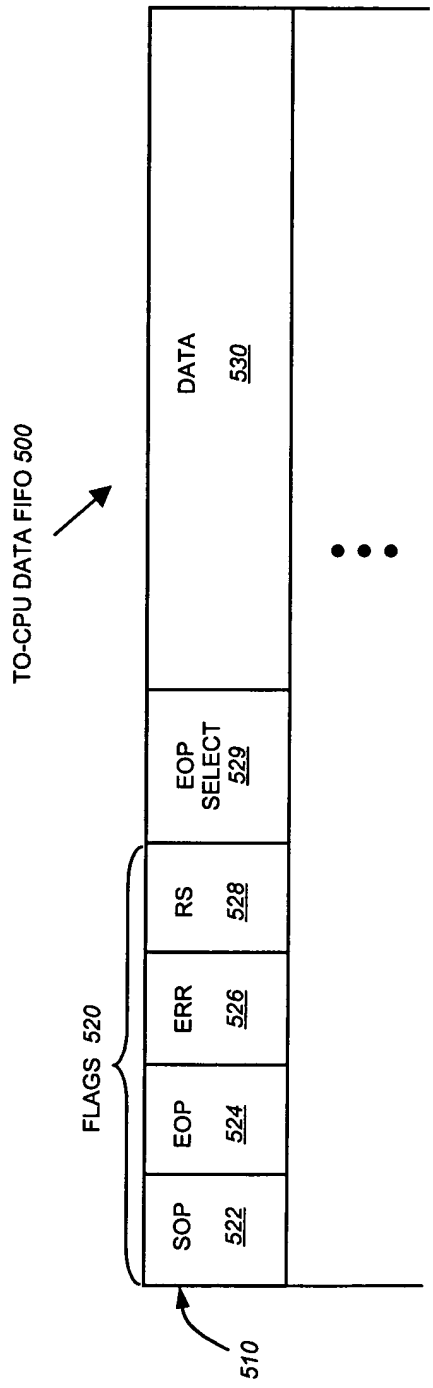

TO-CPU DATA FIFO 500
DATA 530
EOP SELECT 529
RS 528
ERR 526
EOP 524
SOP 522
FLAGS 520
510

FIG. 5

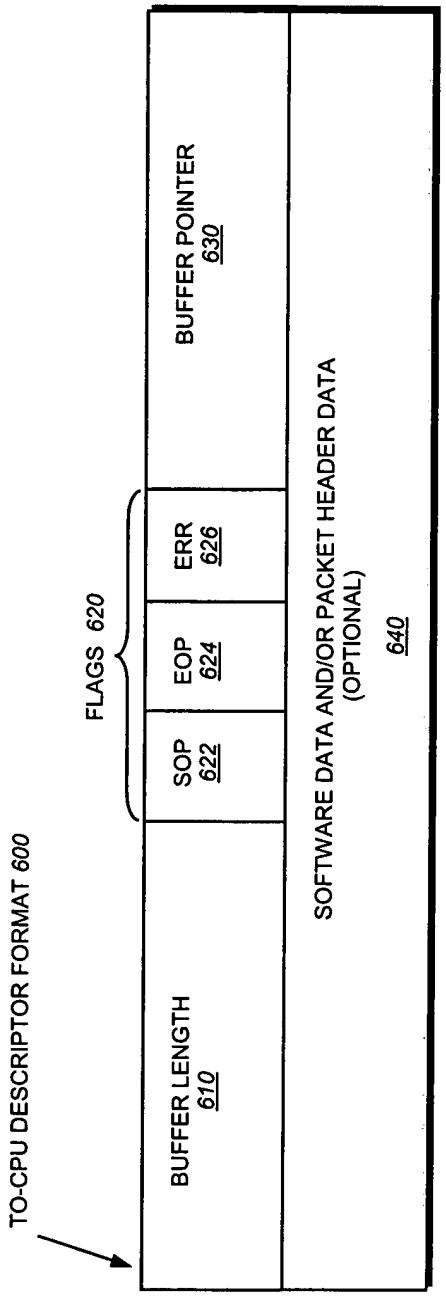

TO-CPU DESCRIPTOR FORMAT 600
BUFFER LENGTH 610
FLAGS 620
SOP 622
EOP 624
ERR 626
BUFFER POINTER 630
SOFTWARE DATA AND/OR PACKET HEADER DATA (OPTIONAL) 640

FIG. 6

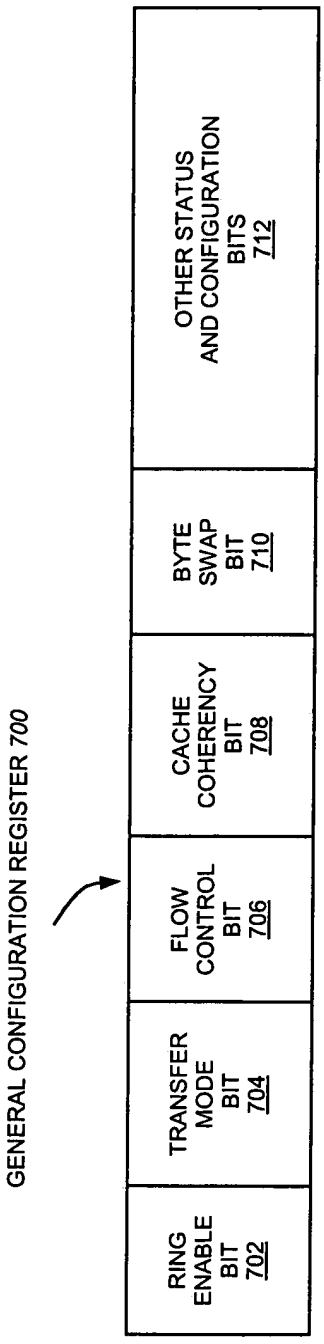
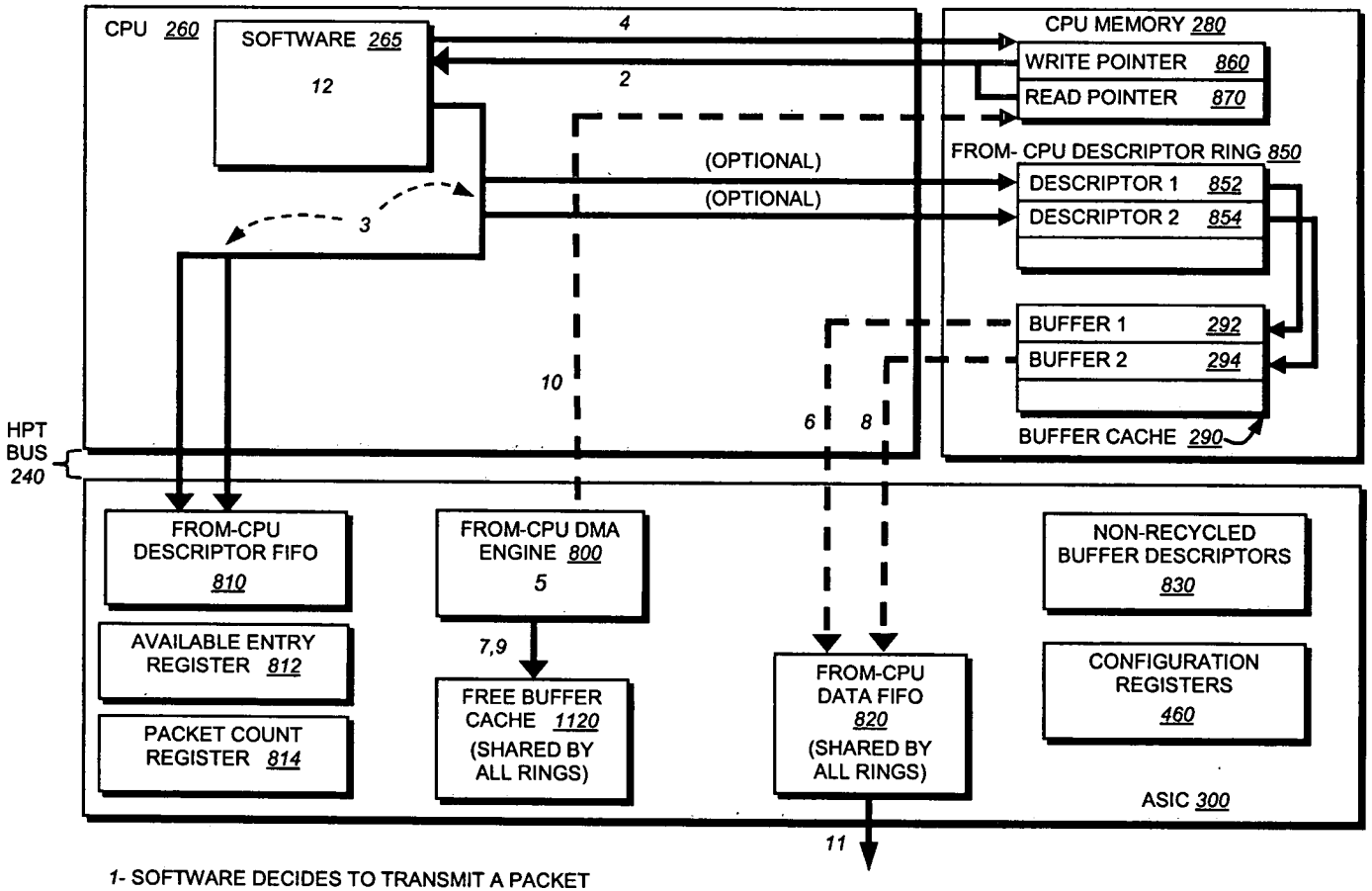

GENERAL CONFIGURATION REGISTER 700
RING ENABLE BIT 702
TRANSFER MODE BIT 704
FLOW CONTROL BIT 706
CACHE COHERENCY BIT 708
BYTE SWAP BIT 710
OTHER STATUS AND CONFIGURATION BITS 712

FIG. 7

FROM-CPU DATA TRANSFER



1- SOFTWARE DECIDES TO TRANSMIT A PACKET
2- SOFTWARE DETERMINES WHETHER SPACE IS AVAILABLE IN THE FROM-CPU DESCRIPTOR FIFO
3- SOFTWARE WRITES DESCRIPTOR(S) TO CPU MEMORY (OPTIONAL) AND TO FROM-CPU DESCRIPTOR FIFO
4- SOFTWARE UPDATES WRITE POINTER
5- DMA ENGINE DETECTS NEW DESCRIPTOR(S) AND ARBITRATES FOR THE FROM-CPU DATA FIFO
6,8- DMA ENGINE COPIES DATA FROM DATA BUFFER TO FROM-CPU DATA FIFO
7,9- DMA ENGINE ADDS BUFFER TO FREE BUFFER POOL IF REUSE BUFFER ENABLE BIT IS SET
10- DMA ENGINE WRITES READ POINTER TO TRANSFER OWNERSHIP OF DESCRIPTORS IF READ POINTER UPDATE FLAG IS SET IN THE DESCRIPTORS
11- PACKET EXTRACTED FROM THE FROM-CPU DATA FIFO

FIG. 8

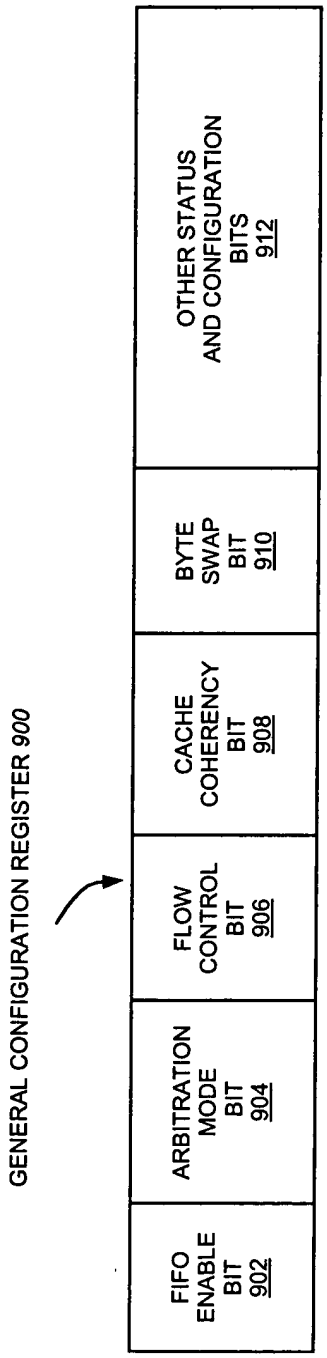

GENERAL CONFIGURATION REGISTER 900
FIFO ENABLE BIT 902
ARBITRATION MODE BIT 904
FLOW CONTROL BIT 906
CACHE COHERENCY BIT 908
BYTE SWAP BIT 910
OTHER STATUS AND CONFIGURATION BITS 912

FIG. 9

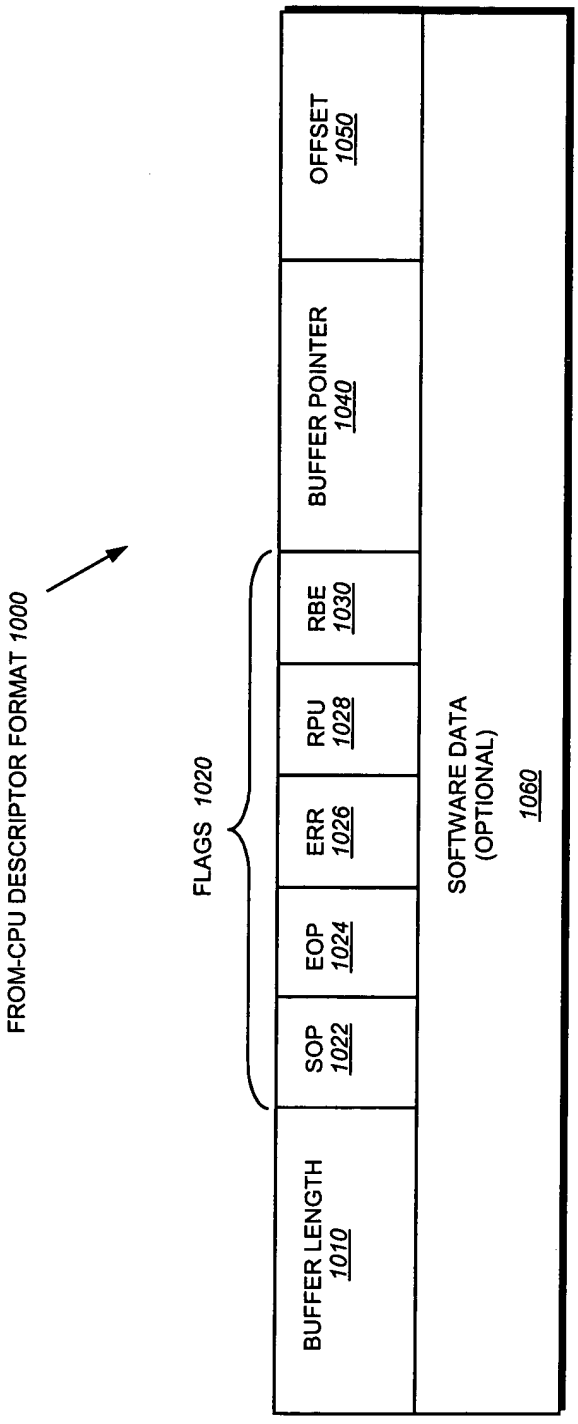

FROM-CPU DESCRIPTOR FORMAT 1000
BUFFER LENGTH 1010
FLAGS 1020
SOP 1022
EOP 1024
ERR 1026
RPU 1028
RBE 1030
BUFFER POINTER 1040
OFFSET 1050
SOFTWARE DATA (OPTIONAL) 1060

FIG. 10

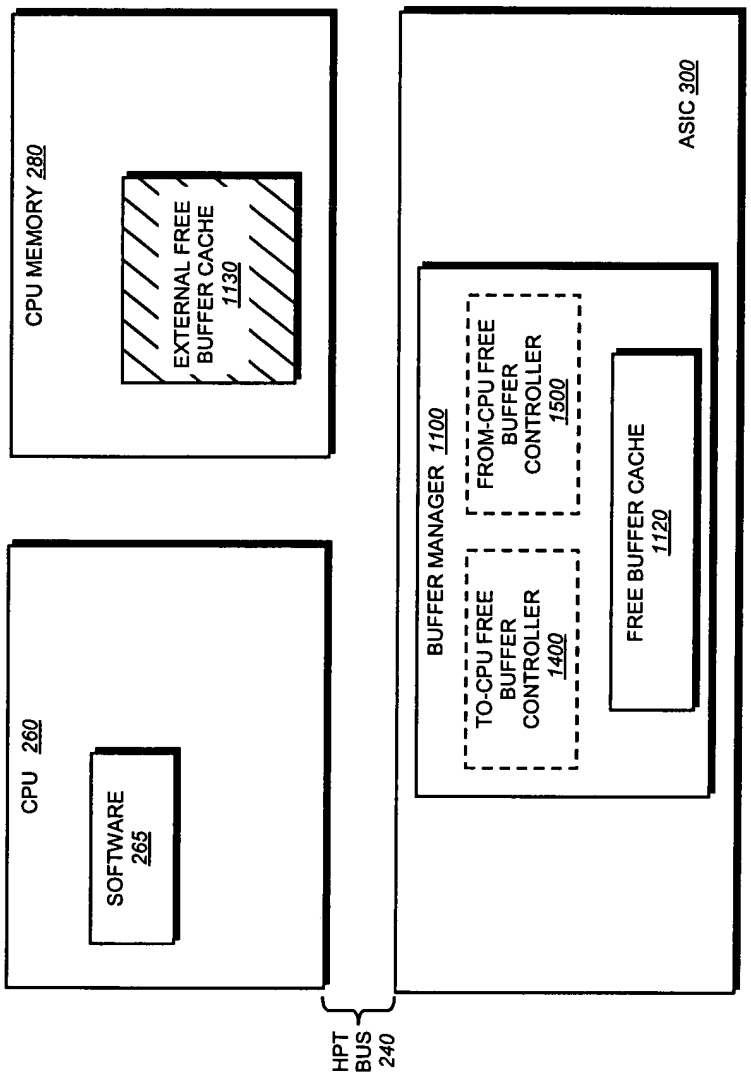

CPU MEMORY 280
EXTERNAL FREE BUFFER CACHE 1130
CPU 260
SOFTWARE 265
HPT BUS 240
ASIC 300
BUFFER MANAGER 1100
TO-CPU FREE BUFFER CONTROLLER 1400
FROM-CPU FREE BUFFER CONTROLLER 1500
FREE BUFFER CACHE 1120

FIG. 11

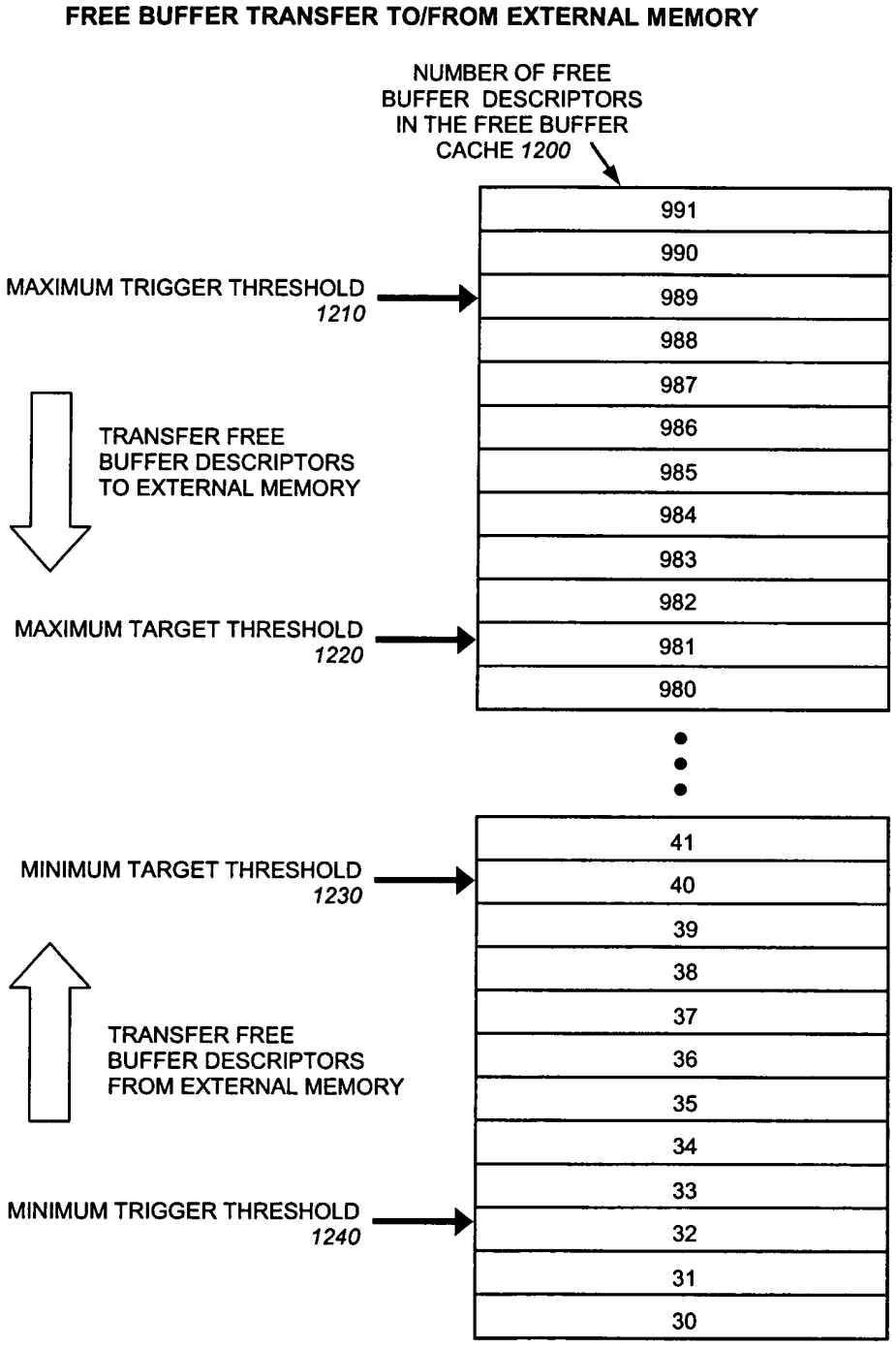

FREE BUFFER TRANSFER TO/FROM EXTERNAL MEMORY
NUMBER OF FREE BUFFER DESCRIPTORS IN THE FREE BUFFER CACHE 1200
991
990
989
988
987
986
985
984
983
982
981
980
MAXIMUM TRIGGER THRESHOLD 1210
TRANSFER FREE BUFFER DESCRIPTORS TO EXTERNAL MEMORY
MAXIMUM TARGET THRESHOLD 1220
41
40
39
38
37
36
35
34
33
32
31
30
MINIMUM TARGET THRESHOLD 1230
TRANSFER FREE BUFFER DESCRIPTORS FROM EXTERNAL MEMORY
MINIMUM TRIGGER THRESHOLD 1240

FIG. 12

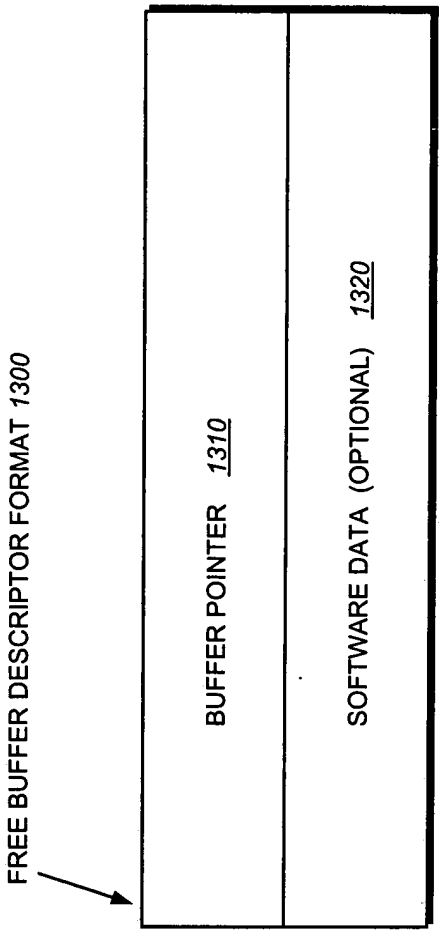
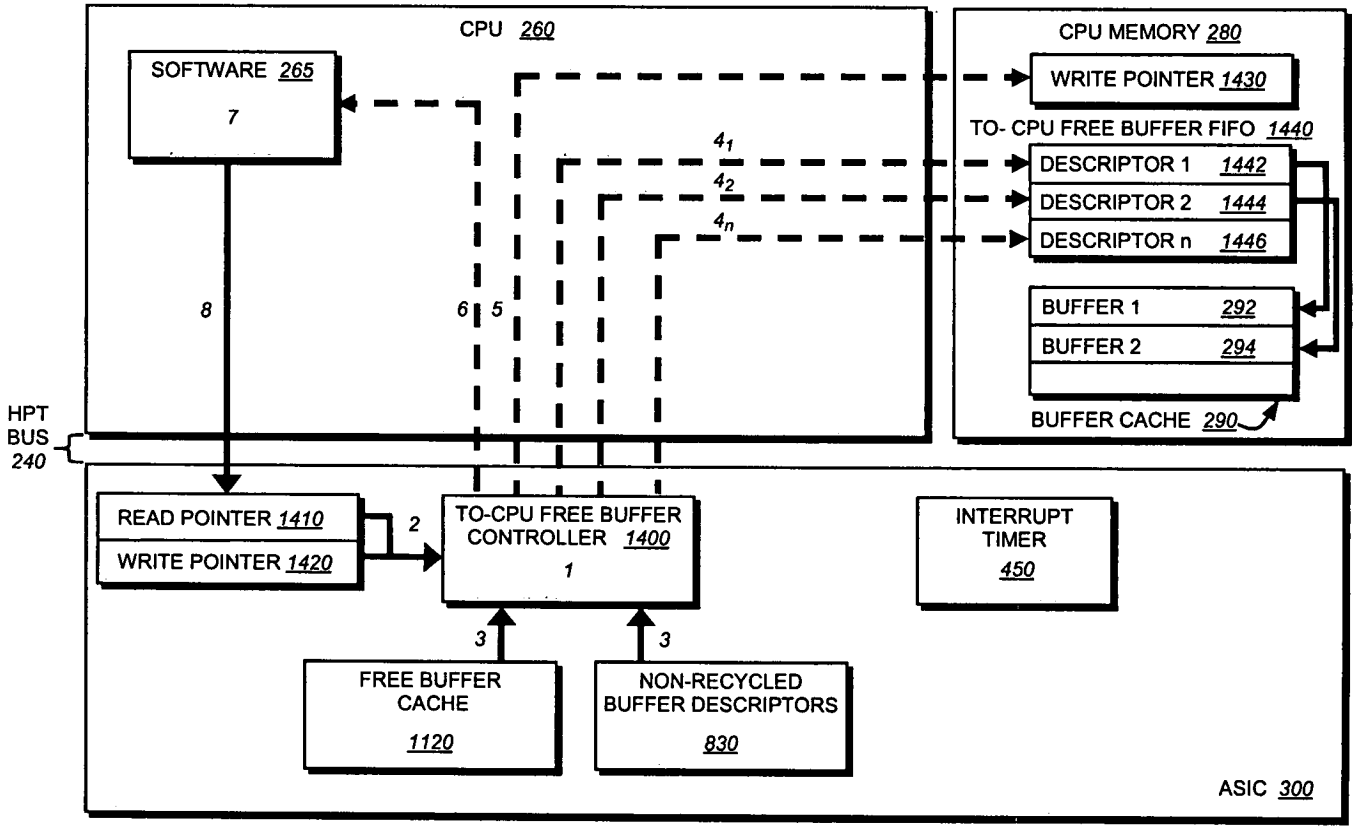

FREE BUFFER DESCRIPTOR FORMAT 1300
BUFFER POINTER 1310
SOFTWARE DATA (OPTIONAL) 1320

FIG. 13

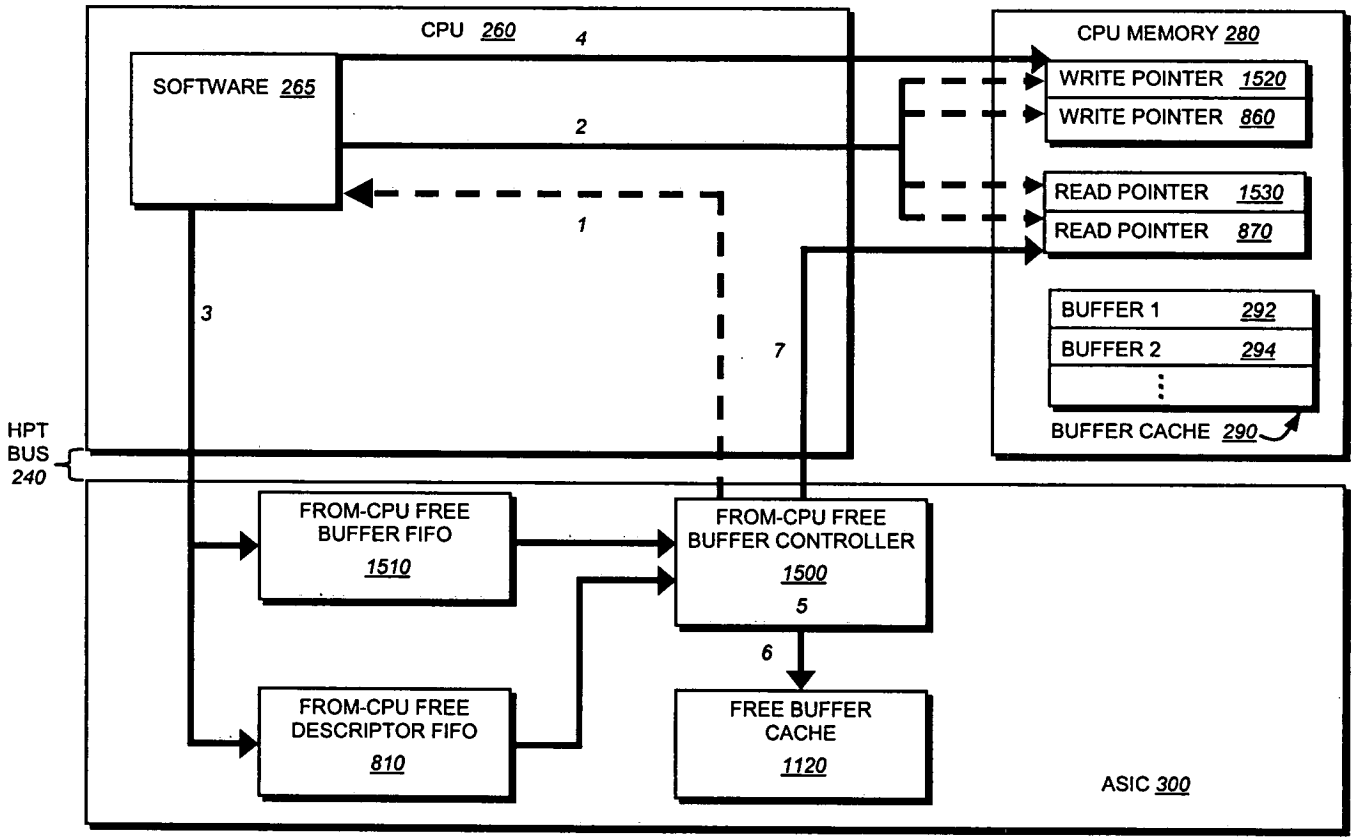
TO-CPU FREE BUFFER TRANSFER



1- FREE-BUFFER CONTROLLER DETERMINES WHETHER FREE BUFFER DESCRIPTOR(S) SHOULD BE TRANSFERRED TO THE CPU
2- FREE-BUFFER CONTROLLER DETERMINES WHETHER ENTRIES ARE AVAILABLE IN THE TO-CPU FREE BUFFER FIFO
3- FREE-BUFFER CONTROLLER ACQUIRES FREE BUFFER DESCRIPTOR(S)
4_{1-n} – FREE-BUFFER CONTROLLER WRITES DESCRIPTORS
5- FREE-BUFFER CONTROLLER WRITES WRITE POINTER AFTER INTERRUPT TIMER EXPIRES
6- FREE-BUFFER CONTROLLER WRITES INTERRUPT
7- SOFTWARE READS A DESCRIPTOR FROM THE TO-CPU FREE BUFFER FIFO
8- SOFTWARE WRITES READ POINTER

FIG. 14

FROM-CPU FREE BUFFER TRANSFER



1- FREE BUFFER CONTROLLER SENDS INTERRUPT TO THE CPU WHEN IT DETERMINES THAT ITS POOL OF FREE BUFFER DESCRIPTORS IS LOW
2- SOFTWARE DETERMINES IF THERE IS AN AVAILABLE ENTRY IN THE FROM-CPU FREE BUFFER FIFO OR FROM-CPU DESCRIPTOR FIFO
3- SOFTWARE WRITES FREE BUFFER DESCRIPTOR
4- SOFTWARE UPDATES APPROPRIATE WRITE POINTER
5- FREE BUFFER CONTROLLER DETECTS NEW FREE BUFFER DESCRIPTOR
6- FREE BUFFER CONTROLLER ADDS DESCRIPTOR TO FREE BUFFER POOL
7- FREE BUFFER CONTROLLER UPDATES APPROPRIATE READ POINTER NEXT TIME A READ POINTER UPDATE FLAG IS DETECTED

FIG. 15